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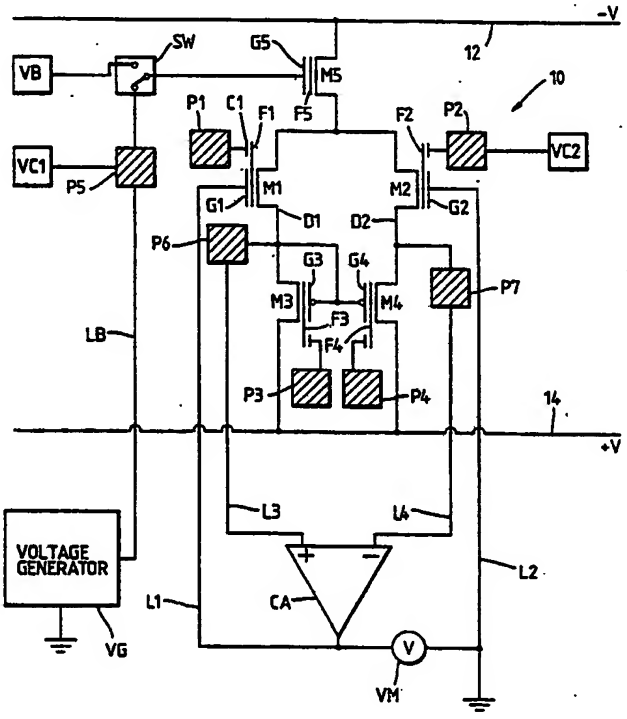
(57) Abstract

A differential amplifier (10) incorporates five metal oxide field effect transistors (MOSFETs) (M1 to M5). The transistors (M1 to M5) are a source-coupled pair of input transistors (M1, M2) with sources connected to a current control transistor (M5) and having respective drain load transistors (M3, M4). The transistors (M1 to M5) have floating gates (F1 to F5) and input gates (G1 to G5). The amplifier (10) is adjusted to counteract differing input transistor threshold voltage by charging one of the input transistor floating gates (G1, G2) to reduce amplifier offset voltage extrapolated to zero input transistor drain current. It is then adjusted to reduce discrepancies between actual and design values of input transistor drain voltage by charging one or both of the drain load transistor floating gates (F3, F4). The amplifier may be arranged as an operational amplifier (20) with a second stage (16) connected to an input transistor drain. The operational amplifier input offset voltage is determined by comparing the second stage output with a reference and feeding a resulting difference signal to the amplifier input. The input offset voltage is then counteracted by charging an input transistor floating gate (F1 or F2) to reduce the difference signal.



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DIFFERENTIAL AMPLIFIER

This invention relates to a differential amplifier and to a method of obtaining an imbalance-corrected differential amplifier.

Differential amplifiers are well known in the prior art. They are based on the so-called long-tailed pair of active three terminal devices. The devices of such a pair have separate input and load connections, but their third terminals are connected together; ie the pair may be a cathode-coupled valve pair, an emitter-coupled bipolar transistor pair or a source-coupled field effect transistor pair. More complex circuits are also known in which a differential amplifier is an input stage of an operational amplifier, and converts two input signals to a single differential signal. In recent years, differential and operational amplifier production has been preferentially based on integrated circuit techniques using complementary metal oxide-silicon (CMOS) technology.

An ideal differential amplifier would have a predetermined output voltage for zero input voltages. It would also have a predetermined output voltage when both input voltages are non-zero but equal; ie the common mode rejection ratio (CMRR) of the amplifier should be infinite. In practice, this ideal is not achieved because of mis-match between component transistors of a differential amplifier.

A differential amplifier has at least one pair of transistors which should ideally be identical. Unfortunately, variations in manufacturing lead to differences between pair members which produce discrepancies between ideal performance and obtained performance.

To improve differential amplifier performance over that obtainable by attention to design and manufacture, it is known to adjust the physical parameters of such amplifiers subsequent to manufacture. One such approach involves incorporating in the amplifier a resistor whose value controls an electrical characteristic of the amplifier. The resistor is made of vaporizable material, and is located in an accessible position

in the amplifier. The resistor is partially vaporized by a laser to alter its resistance to a value appropriate to adjust the amplifier's performance. In practice, a circuit requires robust construction and therefore increased cost to tolerate thermal stresses associated with laser vaporization. Moreover, to achieve adequate performance, it may be necessary to employ more than one vaporizable resistor. The process is limited in accuracy to the minimum change in a resistor value obtainable by a single laser pulse, and is time consuming and expensive.

An alternative approach to differential amplifier adjustment is to replace individual resistors requiring adjustment by respective chains of resistors in series, each resistor being bridged by a Zener diode with associated current terminal pad. One or more individual resistors in each chain may be short-circuited by passing a high reverse current through the associated Zener diodes. The current short-circuits the diode junction, and the chain resistance becomes that due to those remaining resistors which are not short-circuited. Conveniently, the resistor values in a chain form a binary doubling sequence, ie R, $2R,....2^{n-1}R$; seven resistors per chain are needed to achieve resistance adjustment accuracy to 1% of the chain resistance. Moreover, each resistor requires a contact pad. This approach has the disadvantage that part of the circuit is devoted to resistors, contact pads and Zener diodes which are irrelevant to circuit operation after initial circuit adjustment. It is therefore wasteful of integrated circuit material.

It has also been suggested to employ a differential current circuit as a module for insertion in an amplifier to provide current adjustment capability. This is reported by E Sackinger and W Guggenbuhl IEEE J. SC23 1437 (1988), who describe a sub-circuit module suitable for delivering a current of magnitude and polarity required for amplifier adjustment.

An alternative approach has been suggested by L.R. Carley, IEEE J. SC24 1569 (1989). This involves an amplifier with two input field effect transistors each with a drain load transistor in what is known in the

prior art as a "current mirror" arrangement. Carley suggests employing an additional transistor connected in parallel with a drain load transistor and arranged to counteract offset voltage.

All the foregoing prior art techniques for differential amplifier adjustment suffer from the disadvantage that they counteract mis-match by the introduction of asymmetry into the circuit. The traditional long-tailed pair differential amplifier is symmetrical; it has two input circuits which are intended to be identical to one another. The symmetry is lost if resistors and Zener diodes or additional load transistors are used to counteract mis-match. Such prior art techniques allow the amplifier offset voltage to be adjusted and forced to zero for a particular combination of input voltages. However, the average offset voltage over the whole range of amplifier inputs may worsen. That is, the circuit asymmetry degrades the CMRR of the differential amplifier.

It is an object of the invention to provide an alternative form of differential amplifier and a method of adjusting such an amplifier.

The present invention provides a differential amplifier wherein:

(a) a source-coupled pair of transistors are arranged respectively as inverting and non-inverting input transistors of the amplifier,

(b) the input transistors have respective drain load circuits each incorporating a respective subsidiary transistor and the subsidiary transistors forming a pair,

(c) at least one of the pairs of input and subsidiary transistors is a pair of field effect transistors incorporating respective floating gates and

(d) the amplifier includes correcting means for charging at least one of the said floating gates to counteract at least one of:-

(i) differing input transistor threshold voltages, and

(ii) discrepancies between actual and design values of input transistor drain voltage.

The invention provides the advantage that it is a differential amplifier that is adjustable to counteract mis-match without introducing circuit asymmetry as in the prior art. It is adjusted by charging one or more of the amplifier's transistor floating gates, the charge being retained to provide correction for mis-match.

If at least the input transistors are floating gate field effect transistors, the correcting means may be arranged for charging at least an input transistor floating gate to counteract differing input transistor threshold voltages; the amplifier may also include current varying means connected to input transistor sources and arranged to vary input transistor drain currents. The current varying means may comprise a transistor and biasing means arranged to vary the current in that transistor.

The correcting means may include:-

(a) means for controlling the current varying means to determine a linear region of the variation of the amplifier input offset voltage with the square root of the sum of input transistor drain currents, and

(b) means for detecting discrepancies between actual and design values of input transistor drain voltage and for charging at least one of the subsidiary transistor floating gates to counteract such discrepancies.

The amplifier may incorporate one or more transistor floating gates which are chargeable as hereinafter discussed.

The correcting means may include a respective terminal pad connected to the or each floating gate designed for charging, the said terminal pad being connectable to a charging source.

An amplifier of the invention may be arranged as an operational amplifier including a second stage connected to a drain load circuit and the correcting means may include means for charging an input transistor floating gate to counteract amplifier input offset voltage.

In an alternative aspect, the invention provides a method of obtaining a mismatch-adjusted differential amplifier including the steps of:

(a) providing a differential amplifier incorporating a pair of input transistors and a pair of drain load transistors, at least one pair being floating gate field effect transistors, and

(b) charging at least one floating gate of the field effect transistors to counteract at least one of:-

(i) differing input transistor threshold voltages, and

(ii) discrepancies between actual and design values of input transistor drain voltage.

The input transistor threshold voltage difference may be determined by determining the amplifier input offset voltage extrapolated to zero input transistor drain current. The threshold voltage difference is then counteracted by charging an input transistor floating gate as appropriate to produce a reduction therein. Discrepancies between actual and design values of input transistor drain voltage may be determined by providing reference signal levels to the input transistors and monitoring the resulting drain voltages. One or both subsidiary transistor floating gates are then charged to reduce the discrepancies. The amplifier of the invention may be an operational amplifier and may incorporate a second stage connected to an input transistor drain, and the amplifier input

offset voltage may be determined by feeding back to an amplifier input a signal derived by comparing the second stage output with a reference signal level. The offset voltage is then counteracted by charging an input transistor floating gate to reduce it.

The method of the invention is well suited to iteration to achieve successive approximations to required performance. It also lends itself to automation under computer control as employed in conventional integrated circuit testing.

The invention also extends to an operational amplifier made by the foregoing method.

In order that the invention might be more fully understood, an embodiment thereof will now be described with reference to the accompanying drawings, in which:-

Figure 1 is a schematic circuit diagram of a differential amplifier of the invention arranged for determination of input transistor threshold voltage difference and its correction;

Figure 2 is a graph of amplifier offset voltage against gate-source voltage minus threshold voltage of a transistor arranged to control amplifier drain current;

Figure 3 shows the amplifier of Figure 1 arranged for determination and adjustment of discrepancies between actual and design values of amplifier output voltage; and

Figure 4 shows the amplifier of Figures 1 and 3 arranged as part of an operational amplifier in which amplifier input offset voltage is to be corrected.

Referring to Figure 1, there is shown a differential amplifier of the invention indicated generally by 10. The amplifier 10 incorporates first, second, third, fourth and fifth metal oxide-semiconductor field effect transistors (MOSFETs) M1, M2, M3, M4 and M5 produced by CMOS technology. The MOSFETs M1 to M5 are floating gate devices, generally as outlined by S.M. Sze in "Physics of Semiconductor Devices", 2nd Ed. Wiley 1981, page 496. Each MOSFET Mx consequently has two respective gates, a floating gate Fx and an input gate Gx, where x is 1,2,3,4 or 5. Each floating gate Fx is capable of storing electrical charge for a long period. In IEEE Electron Device Letters, Vol.12, No 3, March 1991, Thomsen and Brooke estimate that a floating gate in a silicon MOSFET would lose charge at the rate of 0.1% in 26 years.

The first and second MOSFETs M1 and M2 are the input transistors of the differential amplifier 10. They are NMOS devices, and are connected to form a source-coupled pair (long-tailed pair); the fifth MOSFET M5 is also an NMOS device, and is connected as a common source bias element between the M1/M2 pair and a negative power supply line 12. The third and fourth MOSFETs M3 and M4 are PMOS devices, as indicated conventionally by respective circles adjacent their input gates G3 and G4. These MOSFETs M3 and M4 are drain loads for the first and second MOSFETs M1 and M2 respectively; the connections between associated MOSFETs M1/M3 and M2/M4 are drain to drain. The third and fourth MOSFETs M3 and M4 are connected to a positive power supply line 14, and they act in combination as a current mirror circuit.

A current mirror is a known circuit incorporating a MOSFET with gate and drain terminals connected together. In consequence, the gate-source voltage V_{gs} of such a MOSFET reflects the current through it. Moreover, connection together of the gates G3 and G4 of the third and fourth MOSFETs M3 and M4 ensures that these transistors carry like drain currents when biased to an operating regime where current is independent of drain-source voltage V_{ds} provided that their floating gates F3 and F4 have like charging.

The first to fourth floating gates F1 to F4 have capacitative coupling connections (eg C1) to terminal pads P1 to P4 respectively. The fifth MOSFET floating gate F5 has no associated pad. The first and second pads P1 and P2 are connected to respective charging voltage sources VC1 and VC2.

The first and second input gates G1 and G2 are connected by first and second lines L1 and L2 to respective sides of a voltmeter VM. The line L2 is also connected to earth. The third and fourth MOSFET input gates G3 and G4 are connected directly together as has been said. The fifth MOSFET input gate G5 is connected to a single pole, double throw switch SW having poles connected to a bias voltage source VB and to a terminal pad P5. The pad P5 is connected by a line LB to a DC voltage generator VG.

The first and second MOSFETs M1 and M2 have drain connections D1 and D2 connected both to the third and fourth MOSFETs M3 and M4 and to terminal pads P6 and P7 respectively. The pads P6 and P7 are also connected by lines L3 and L4 as input terminals of a comparator amplifier CA.

The differential amplifier 10 is adjusted as follows to correct for differing threshold voltages V_{T1} and V_{T2} of the first and second MOSFETs M1 and M2. The switch SW is set to connect the fifth input gate G5 to the terminal pad P5 and thence to the voltage generator VG. The charging voltage sources VC1 and VC2 are initially isolated (not shown) from the pads P1 and P2. The drain current of the fifth MOSFET M5, and consequently that of each of the first and second MOSFETs M1 and M2, is adjusted by means of the voltage generator VG until the first and second MOSFETs are operating in a saturation regime.

The comparator amplifier CA receives input of the drain voltages of the first and second MOSFETs M1 and M2; it amplifies the difference between these voltages. The amplified difference voltage is fed back to the first input gate G1 with a polarity appropriate to reduce the difference between the first and second MOSFET drain voltages. When feedback has

produced a quiescent state, the output voltage from the comparator amplifier CA is that input voltage to the differential amplifier 10 which produces equality between the drain voltages of the first and second MOSFETs M1 and M2; this input voltage is defined as the offset voltage V_{OS}, and it is shown by the voltmeter VM.

The difference δV_{T12} between the threshold voltages V_{T1} and V_{T2} of the first and second MOSFETs M1 and M2 is determined by a graphical extrapolation technique. When δV_{T12} has been determined, it is reduced by applying a charge of the appropriate polarity to one of the first and second floating gates F1 and F2 by means of the respective charging voltage sources VC1 or VC2. The graphical and charging techniques are described in more detail below. The reduced value of δV_{T12} is determined by the graphical technique once more, and is further reduced by altering the charge previously applied to the floating gate F1 and F2. The procedure is repeated iteratively until the residual value of δV_{T12} is sufficiently small to be negligible for the purpose for which the amplifier 10 is intended.

The graphical extrapolation technique referred to above is derived as follows: the offset voltage V_{OS} (shown on the voltmeter VM in Figure 1) has been analysed for a source-coupled pair of MOSFETs by P R Gray and R G Meyer in "Analysis and Design of Analog Integrated Circuits", Second Edition, John Wiley and Sons 1984. From that analysis, it can be shown that, if the first, second and fifth MOSFETs M1, M2 and M5 are operating in saturation, then approximately:-

$$V_{OS} = \delta V_{T12} + A[I_{D5}]^{\frac{1}{2}} \qquad (1)$$

where I_{D5} is the drain current of the fifth MOSFET M5, and A is a constant. Equation (1) is an approximate relationship which arises because V_{OS} is related to the drain currents of the first and second MOSFETs M1 and M2, and these currents are approximately equal to each other and to $I_{D5}/2$.

$$\text{However, in saturation, } I_{D5} \propto [V_{GS5} - V_{T5}]^2 \qquad (2)$$

where V_{GS5} and V_{T5} are the fifth MOSFET's gate-source voltage and threshold voltage respectively.

Combining (1) and (2):-

$$V_{OS} = \delta V_{T12} + B(V_{GS5} - V_{T5}) \qquad (3)$$

where B is a constant.

Equation (3) shows that the variation of V_{OS} as a linear function of the square root $[I_{D5}]^{\frac{1}{2}}$ of the sum of the first and second MOSFETs' drain currents can be replaced by a like variation with $(V_{GS5} - V_{T5})$.

A typical value for a MOSFET threshold voltage V_T is 0.85V, and this value may be employed to replace V_{T5} in Equation (3) with a degree of error that is negligible.

V_{GS5} is the voltage difference between the voltages on the line LB and the negative power supply line 12, and is controlled by the voltage generator VG. As has been said, V_{OS} is measured by the voltmeter VM. From Equation (3), a graph of V_{OS} against $(V_{GS5} - V_{TS})$ produces a straight line of slope B. This line has an intercept on the V_{OS} axis of δV_{T12}, the difference between the threshold voltages V_{T1} and V_{T2} of the first and second MOSFETs M1 and M2. The graph is produced by connecting the fifth

MOSFET gate G5 to the voltage generator VG, varying the generator output voltage. This produces a variation in V_{OS} on the voltmeter VM.

Referring now also to Figure 2, there is shown a graph 15 of V_{OS} against $(V_{GS5} - V_{T5})$. The graph has a linear portion 15A and a curved portion 15B; the latter arises from departures from the assumptions on which Equations (1) to (3) were based. The linear portion 15A is extrapolated by a chain line 15C to an intercept δV_{T12} of -18.7mV on the V_{OS} axis. The graph 15 indicates that the first MOSFET M1 has a threshold voltage V_{T1} 18.7mV below that of the second MOSFET M2.

In order to counteract the threshold voltage difference, a charge is applied to one of the floating gates F1 and F2 and the procedure used to generate the graph 15 is repeated. If the value of δV_{T12} increases, the polarity of the charge is reversed and the procedure repeated. If δV_{T12} is reduced, the procedure is repeated with a charge of like polarity and lesser or greater magnitude in accordance with whether the reduction was greater than or less than $\frac{1}{2}\delta V_{T12}$. Successive iterations of this procedure provide a negligible residual threshold voltage difference.

Charge is introduced on to the relevant floating gate F1 or F2 as described by A Thomsen and M A Brooke, IEEE Electron Device Letters, Vol. 12, No. 3, March 1991. The terminal pads P1 to P4 are capacitatively coupled to respective floating gates F1 to F4; each capacitative coupling is however constructed as a charge injector as described by Thomsen et al. In consequence, a voltage on one of the pads P1 to P4 produces the injection of charge on to the associated gate F1, F2, F3 or F4. The charge remains on the relevant gate after the voltage is removed from the associated pad, and persists for a considerable time as has been said.

Referring now to Figure 3, there is shown the differential amplifier 10 of Figure 1 with changes to subsidiary circuitry for the purposes of determining charges to be applied to the third and fourth MOSFETs M3 and M4. Parts previously described are like referenced. The differential

amplifier 10 has first and second input gates G1 and G2 connected to earth. The terminal pads P6 and P7 are connected to first and second voltmeters VM1 and VM2 respectively, which are also connected to earth. Terminal pad P5 is unconnected. The third and fourth terminal pads P3 and P4 are connected to a variable voltage source VS. The switch SW is set to connect the fifth input gate G5 to the bias voltage source VB.

The voltage source VS is employed to apply voltages to the third and fourth pads P3 and P4, so that charges are injected on to the third and fourth floating gates F3 and F4. This alters the drain voltages of the first and second MOSFETS M1 and M2 to respective predetermined values for which the amplifier 10 was designed. The drain voltages appear at the sixth and seventh pads P6 and P7 respectively, and are measured by the first and second voltmeters VM1 and VM2. When the predetermined values are achieved, the voltage source VS is disconnected from the pads P3 and P4. This leaves charges on third and fourth floating gates appropriate for maintaining the design values of the first and second MOSFET drain voltages.

Referring now to Figure 4, there is shown the differential amplifier 10 arranged as an input stage of an operational amplifier 18 having a second stage 16. The second stage 16 has an output 20 connected as one input to a comparator amplifier CA1. A voltmeter VM3 is connected between earth and an output CAO of the comparator amplifier CA1, and this amplifier has earth as a second input. The amplifier output CAO is connected to the second input gate G2. A voltage source VS1 is connected to the first floating gate terminal pad P1. The first input gate G1 is connected to earth.

The circuit of Figure 4 operates as follows. The first input gate G1 is at earth potential. The signal at the second drain connection D2 is connected to the second stage 16. The output signal from the second stage 16 is compared with earth potential in the comparator amplifier CA1. Output from the comparator amplifier CAO is fed to the second input gate G2, and has a polarity appropriate to reduce the output voltage appearing

at the operational amplifier output 20. In consequence, negative feedback takes place in the loop defined by the differential amplifier 10, the second stage 16 and the comparator amplifier CA1. When this feedback loop stabilises, the output voltage of the comparator amplifier CA1 is that which is necessary to produce a zero voltage at the operational amplifier output 20. This comparator output voltage is the systematic input offset voltage of the two-stage operational amplifier 18 determined over both amplifier stages 10 and 16. It appears displayed on the voltmeter VM3. To adjust the operational amplifier 18 for zero systematic input offset voltage, either the first floating gate F1 or alternatively the second floating gate F2 is charged as appropriate to reduce the voltage shown on the voltmeter VM3. The procedure involving charge injection is iterative and equivalent to that described with reference to Figure 1.

The invention lends itself to automation of the kind employed for conventional integrated circuit testing. Thus the terminal pads P1 to P7 may be designed to accept probes linked to a computer with associated voltage sources and measuring devices, the computer being programmed to implement supply and detection of voltages and to activate floating gate charging. Such an arrangement is well suited to iterative procedures and to adjustment of arrays of amplifiers.

The current mirror drain load circuit of the differential amplifier 10 may be replaced by any other drain load circuit having a respective floating gate transistor for each input transistor. Variation of the drain currents of the first and second MOSFETs M1 and M2 may be achieved by a current source connected in parallel with a bias element such as the fifth MOSFET M5, the source being disconnectable after adjustment of δV_{T12} to a low value.

The invention has been described with reference to adjustment to counteract differing threshold voltages and departures from design values of input transistor drain voltages, and also input offset voltage when the differential amplifier is part of an operational amplifier. However,

in individual applications of the invention not all of these adjustments may be required. Any one, any two or all three might be appropriate according to circuit design requirements in specific circumstances. In some operational amplifier applications in particular input voltage offset adjustment may be unnecessary.

The differential amplifier 10 incorporated a respective terminal pad (eg P1) for each of the four MOSFETs M1 to M4. It would be possible for the invention to be implemented with only one of the first and second MOSFETs M1 and M2 having a terminal pad. Since a floating gate may be charged positive or negative, a correction requiring a positive charge on floating gate F1 may be implemented by a negative charge on floating gate F2. However, this introduces circuit design asymmetry which might not be acceptable.

CLAIMS

1. A differential amplifier wherein:

(a) a source-coupled pair of transistors are arranged respectively as inverting and non-inverting input transistors of the amplifier,

(b) the input transistors have respective drain load circuits each incorporating a respective subsidiary transistor and the subsidiary transistors forming a pair,

(c) at least one of the pairs of input and subsidiary transistors is a pair of field effect transistors incorporating respective floating gates, and

(d) the amplifier includes correcting means for charging at least one of the said floating gates to counteract at least one of:-

(i) differing input transistor threshold voltages, and

(ii) discrepancies between actual and design values of input transistor drain voltage.

2. An amplifier according to Claim 1 wherein the correcting means is arranged for charging at least an input transistor floating gate to counteract differing input transistor threshold voltages, and wherein the amplifier includes current varying means connected to the input transistor sources and arranged to vary the input transistors' drain currents.

3. An amplifier according to Claim 2 wherein the current varying means comprises a transistor and biasing means arranged to vary the current in that transistor.

4. An amplifier according to Claim 2, or 3 wherein the correcting means includes:

(a) means for controlling the current varying means to determine a linear region of the variation of the amplifier offset voltage with the square root of the sum of input transistor drain currents, and

(b) means for detecting discrepancies between actual and design values of input transistor drain voltage and for charging at least one of the subsidiary transistor floating gates to counteract such discrepancies.

6. An amplifier according to any preceding claim wherein the correcting means includes a respective terminal pad connected to the or each floating gate designed for charging, the said terminal pad being connectable to a charging source.

7. An amplifier according to any preceding claim arranged as an operational amplifier including a second stage connected to a drain load circuit, the correcting means including means for charging an input transistor floating gate to counteract amplifier input offset voltage.

8. A method of producing a mismatch-adjusted differential amplifier including the steps of:-

(a) providing a differential amplifier incorporating a pair of input transistors and a pair of drain load transistors, at least one pair being floating gate field effect transistors, and

(b) charging at least one floating gate of the field effect transistors to counteract at least one of:-

(i) differing input transistor threshold voltages, and

(ii) discrepancies between actual and design values of input transistor drain voltage.

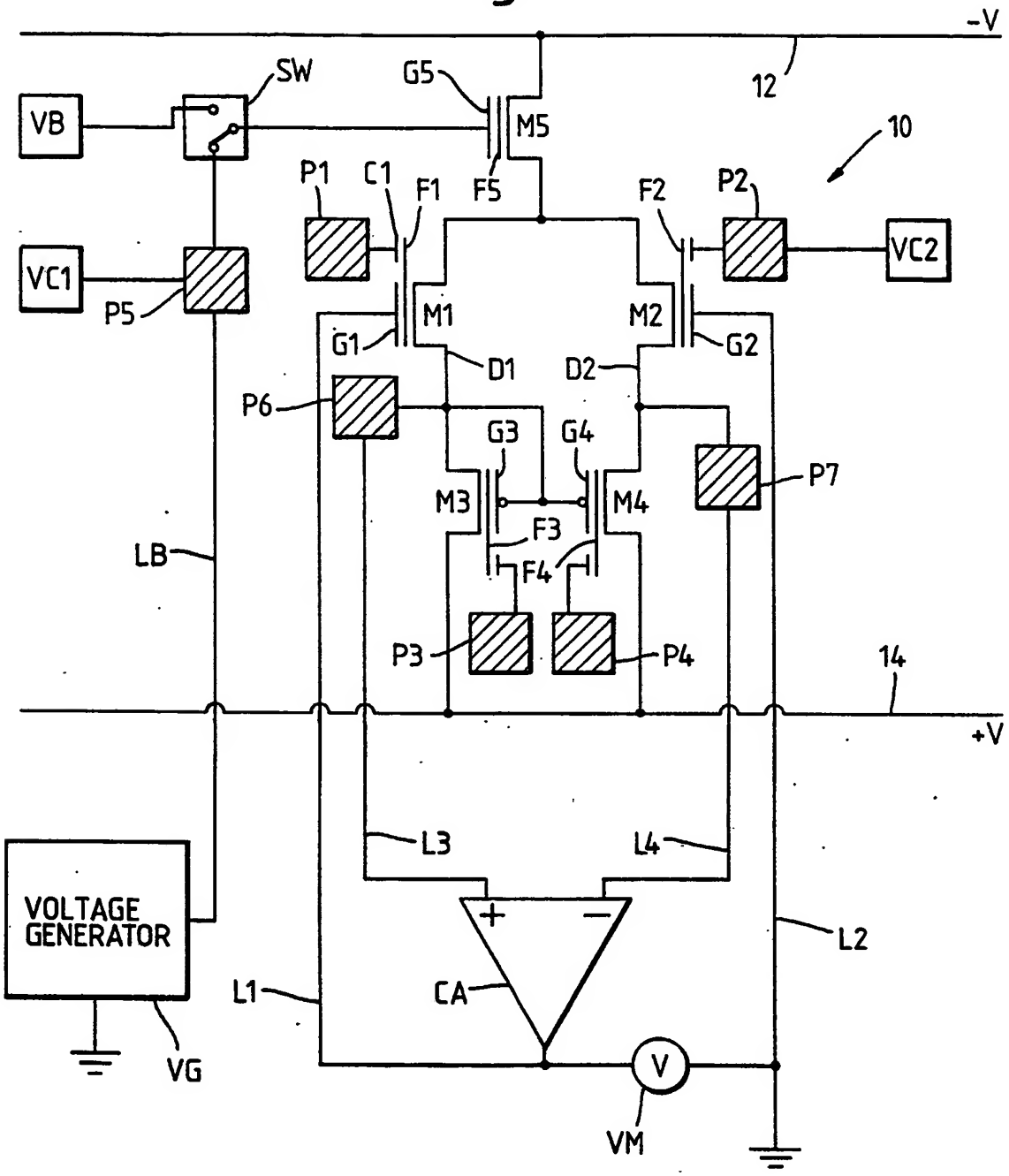
9. A method according to Claim 8 wherein prior to step (b) the input transistor threshold voltage difference is determined by measuring the amplifier input offset voltage as a linear function of the square root of the sum of the input transistor drain currents and extrapolating that voltage to zero drain current sum, and step (b)(i) is implemented by charging an input transistor floating gate.

10. A method according to Claim 8 or 9 wherein step (b)(ii) is carried out, the said discrepancies are determined by providing reference signal levels to the input transistors and monitoring the input transistor drain voltages which result, and at least one of the subsidiary transistor floating gates is charged to counteract any such discrepancy.

11. A method according to Claim 8, 9 or 10 wherein the amplifier has a second stage connected to an input transistor drain, amplifier input offset voltage is determined by feeding back to an amplifier input a signal derived by comparing the second stage output with a reference signal level, and this offset voltage is counteracted by charging an input transistor floating gate to reduce it.

12. An operational amplifier produced by the method of any one of Claims 5 to 8.

Fig.1.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VB
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P1
C1
F1
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F2
P2
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VC1
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M2
G1
G2
D1
D2
P6
G3
G4
P7
M3
M4
F3
LB
F4
P3
P4
14
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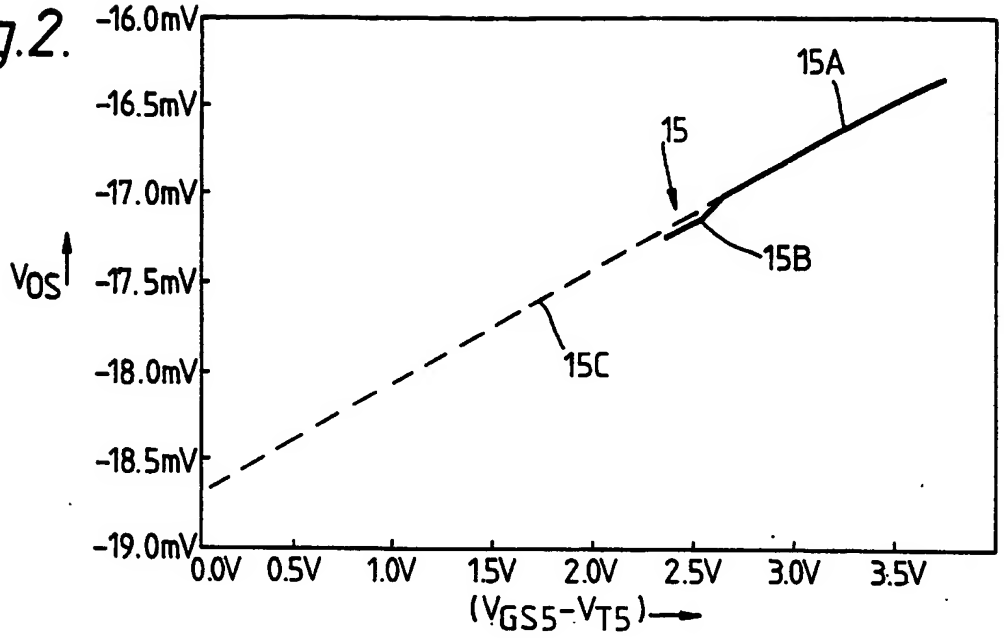
VOLTAGE GENERATOR
L2
L1
CA
V
VG
VM

Fig.2.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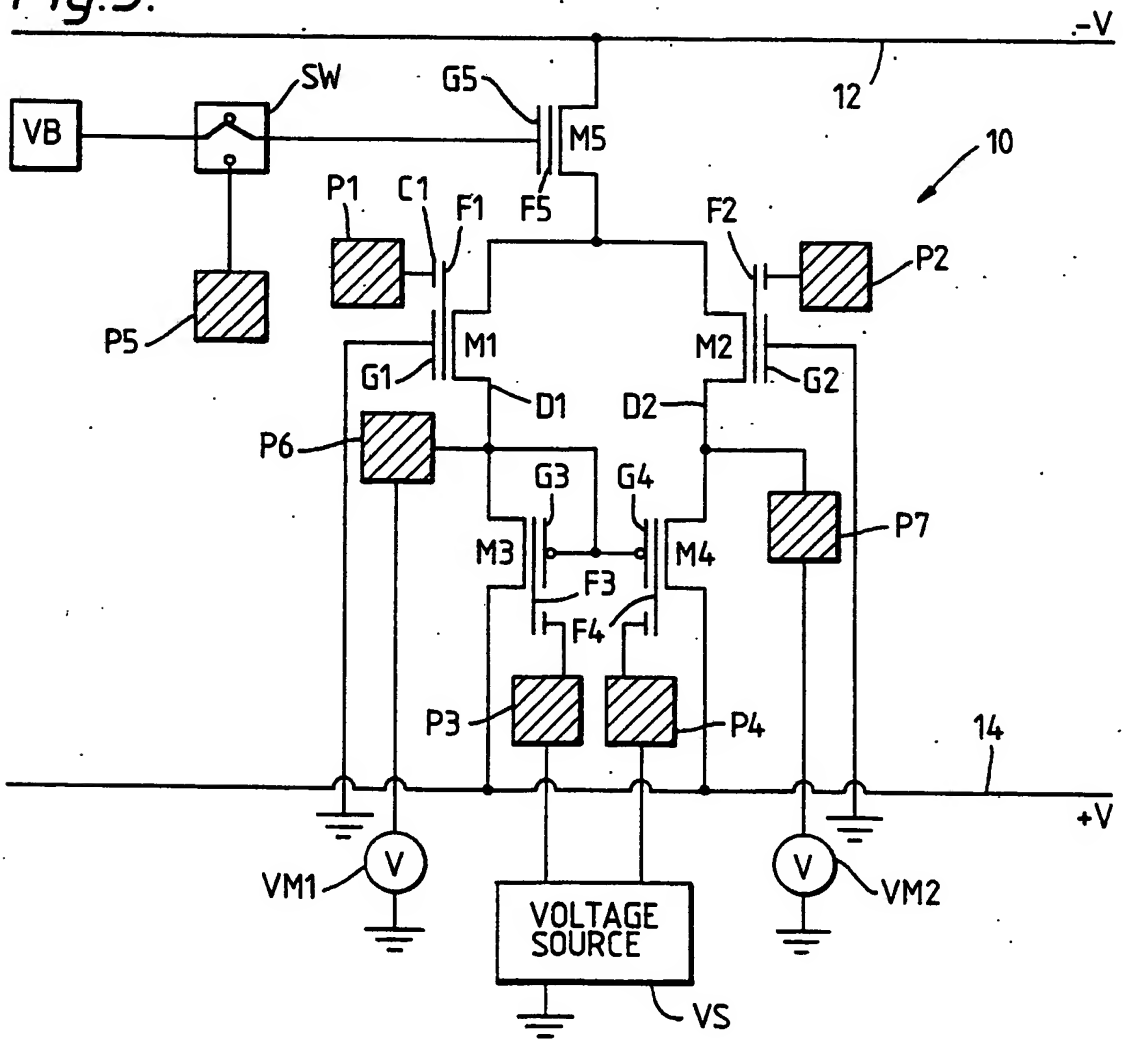
-17.0mV
-17.5mV
-18.0mV
-18.5mV
-19.0mV
VOS
0.0V 0.5V 1.0V 1.5V 2.0V 2.5V 3.0V 3.5V
(VGS5-VT5)
15A
15
15B
15C

Fig.3.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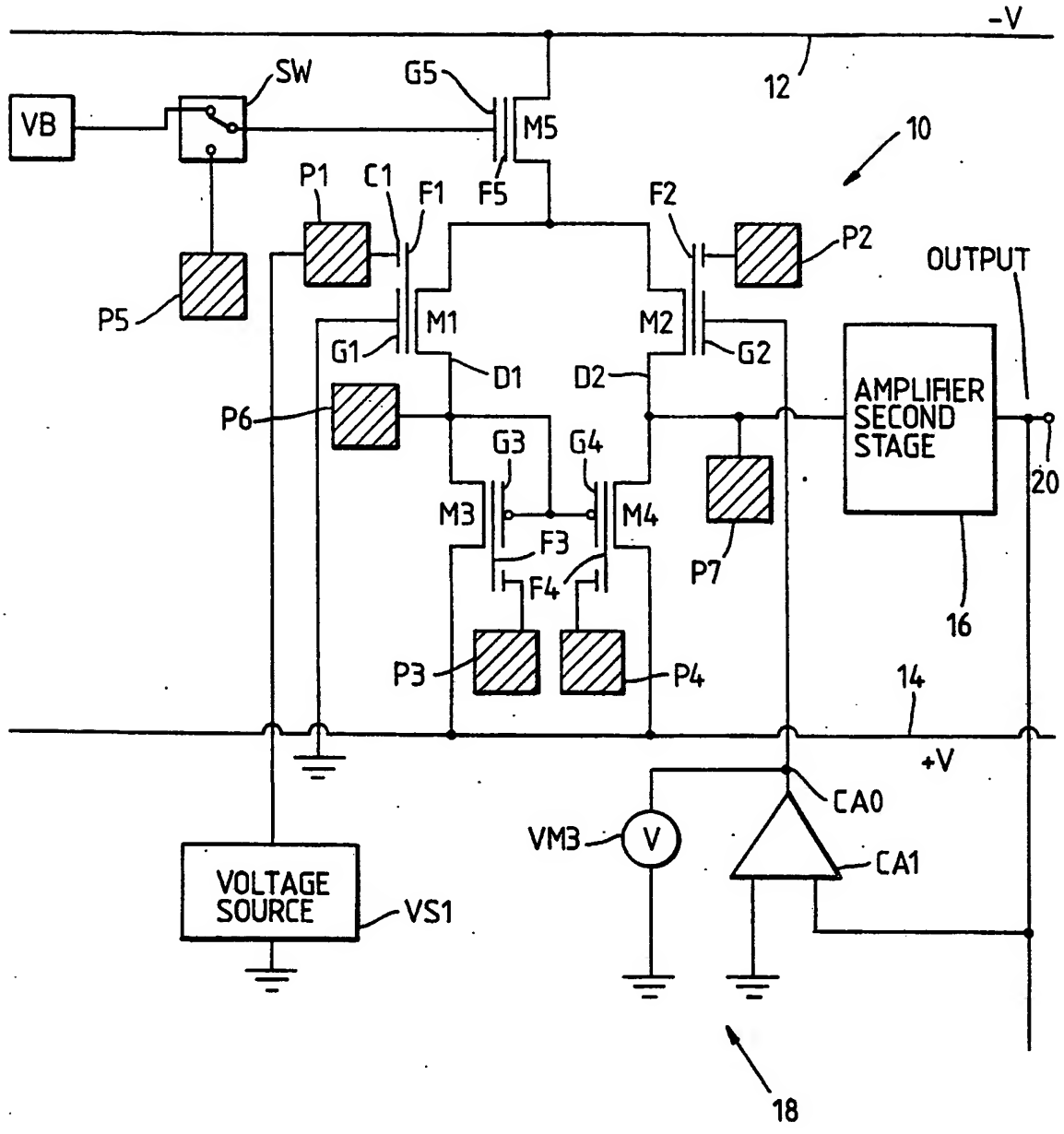
P4
14
+V
VM1
V
VOLTAGE SOURCE
V
VM2
VS

Fig.4.


-V
12
SW
G5
VB
M5
10
P1
C1
F1
F5
F2
P2
OUTPUT
P5
M1
M2
G1
G2
D1
D2
AMPLIFIER SECOND STAGE
P6
G3
G4
20
M3
M4
F3
F4
P7
16
P3
P4
14
+V
CA0
VM3
V
CA1
VOLTAGE SOURCE
VS1
18

INTERNATIONAL SEARCH REPORT

International Application No PCT/GB 93/00311

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all)[6]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int.Cl. 5 H03F3/45

II. FIELDS SEARCHED

Minimum Documentation Searched[7]

Classification System	Classification Symbols
Int.Cl. 5	H03F

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched[8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT[9]

Category °	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No.[13]
X	FR,A,2 543 363 (E.F.C.I.S. -FR) 28 September 1984	1,8
A	see the whole document	2-7,9-12
X	EP,A,0 395 894 (KABUSHIKI KAISHA TOSHIBA) 7 November 1990	1,8
A	see the whole document	2,9

° Special categories of cited documents : [10]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
28 MAY 1993	07.06.93
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	TYBERGHIEN G.M.

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON INTERNATIONAL PATENT APPLICATION NO.

GB 9300311
SA 70200

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report.
The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information. 28/05/93

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
FR-A-2543363	28-09-84	None	
EP-A-0395894	07-11-90	US-A- 5021693	04-06-91

EPO FORM P0479

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82